A 0.35-V 5,200-μm^2 2.1-MHz Temperature-Resilient Relaxation Oscillator with 667fJ/cycle Energy Efficiency Using Asymmetric Swing-Boosted RC Network and Dual-Path Comparator

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Outline

- Introduction
- Theoretical Analysis
- Proposed Architecture
- Measurement Results
- Conclusion

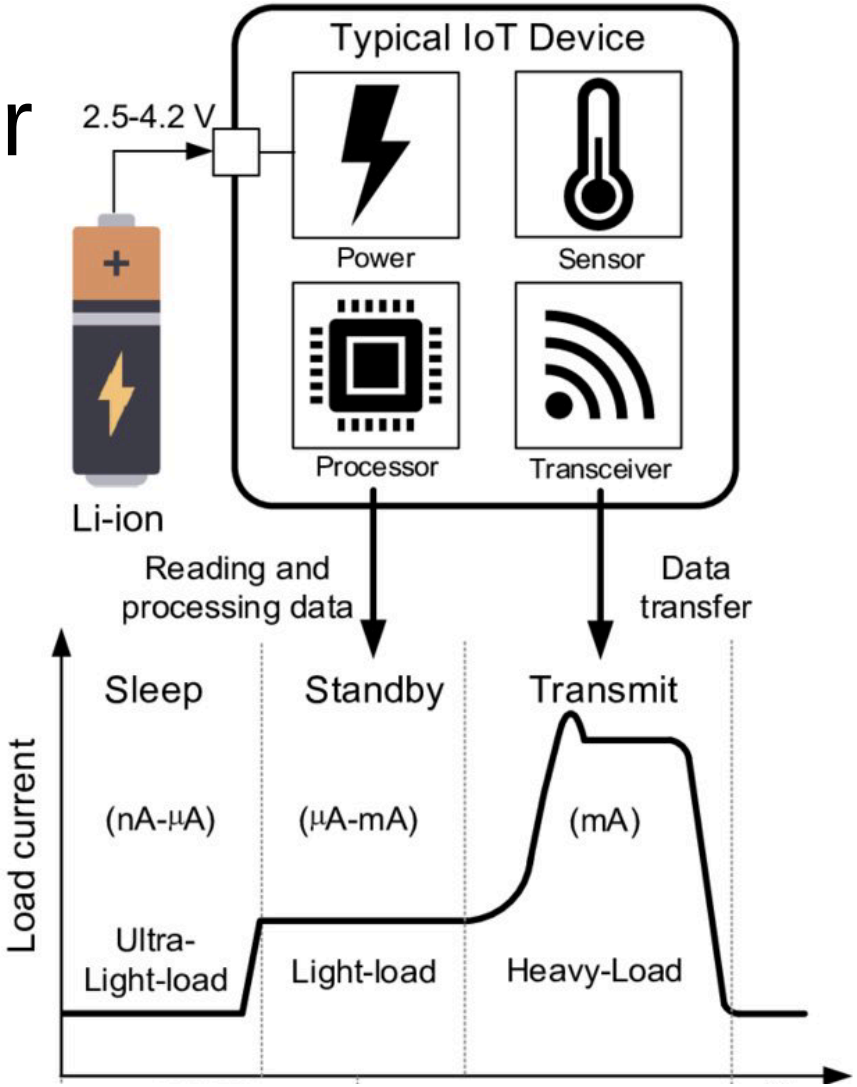
Duty-Cycling in ULP Radios for Power Saving

- Duty-cycling the device to save power
  - As low as 0.1%
- To effectively achieve duty-cycling:
  - Accurately wake up the device
  - Low-power in sleep mode

$$E_{TOTAL} = P_{TRX} \times T_{ON} + P_{SLEEP} \times T_{OFF}$$

- Two methods to wake the device up
  - Timer
  - Wakeup receiver

Fully-integrated timer for miniaturization



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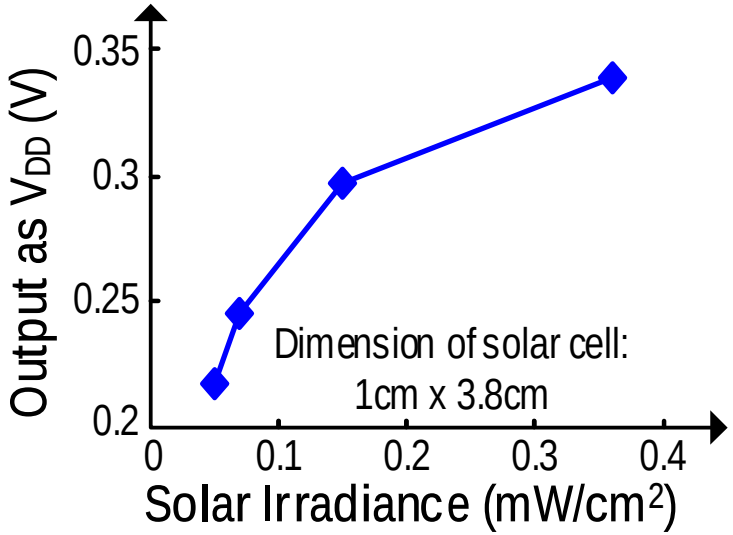
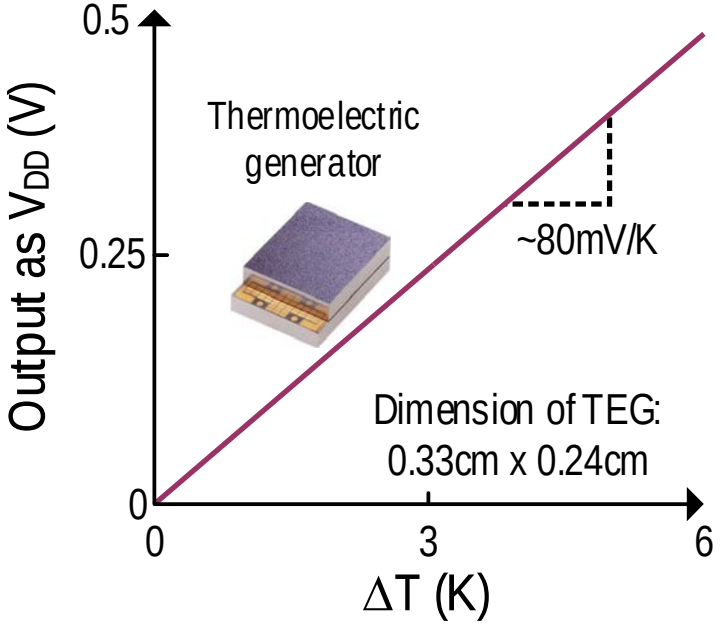
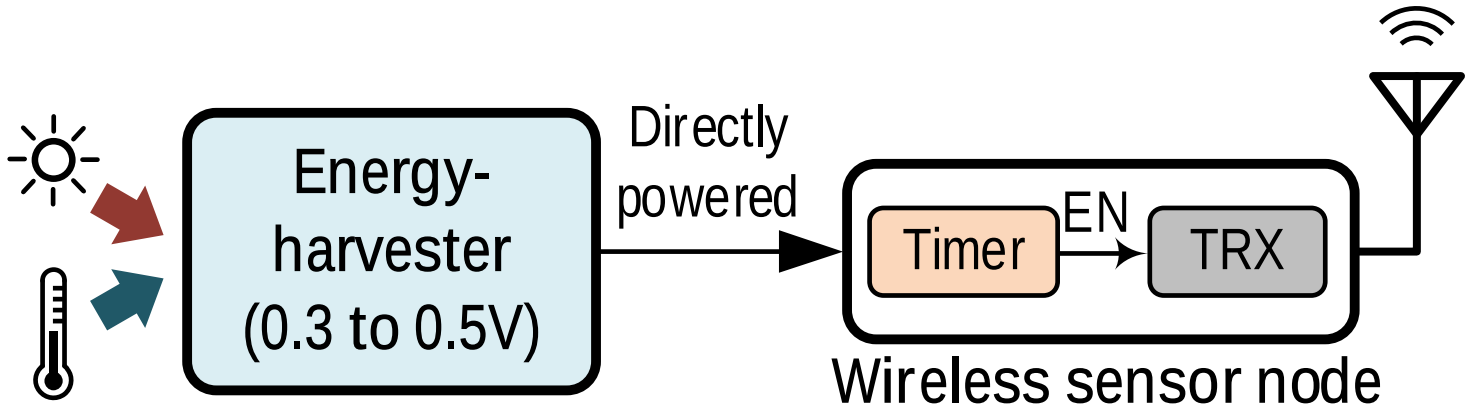
Energy-Harvesting for Self-Sustainability





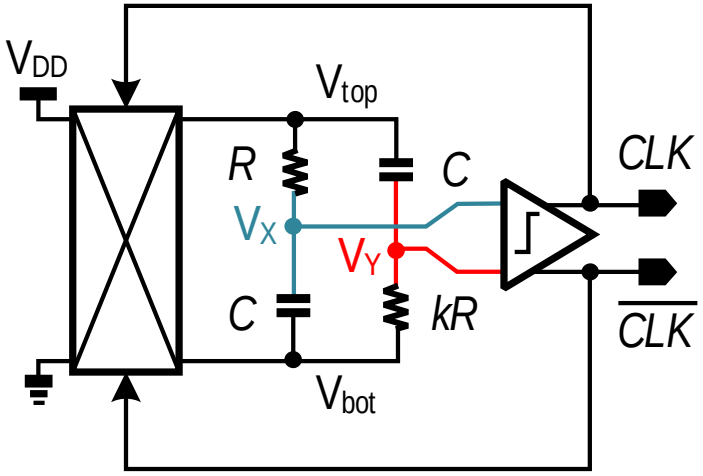
- Energy harvesting for perpetual operation
- Interim DC-DC converters incur power loss & cost



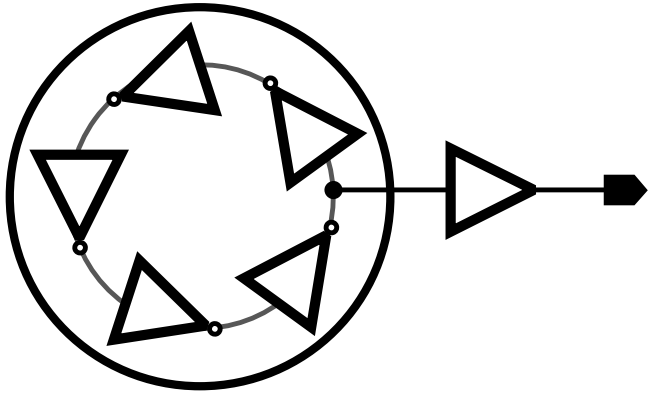
- ***Key Challenge*: to operate at a sub-0.5V, i.e. ultra-low-voltage (ULV)?**

Architecture of Fully-Integrated Timer

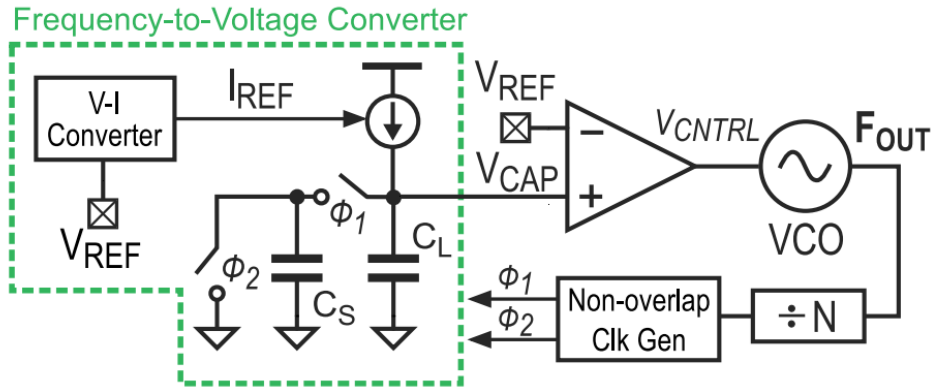
Relaxation Oscillator (RxO)



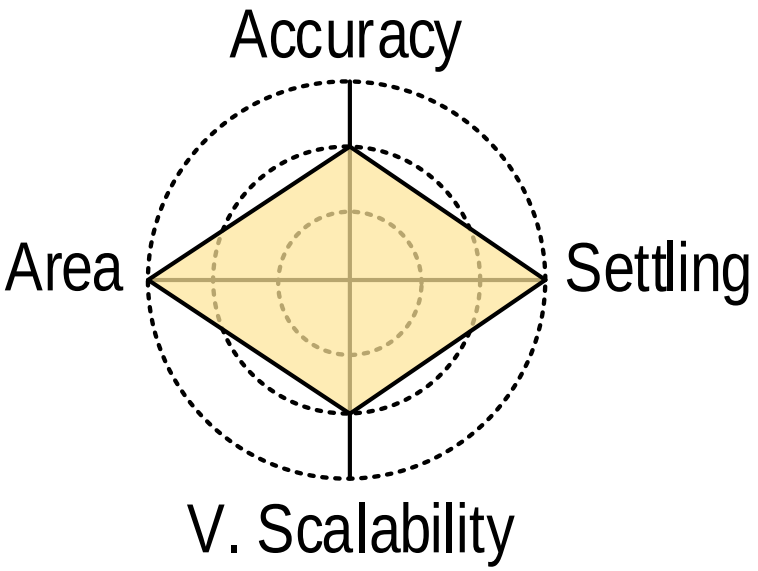
Ring Oscillator

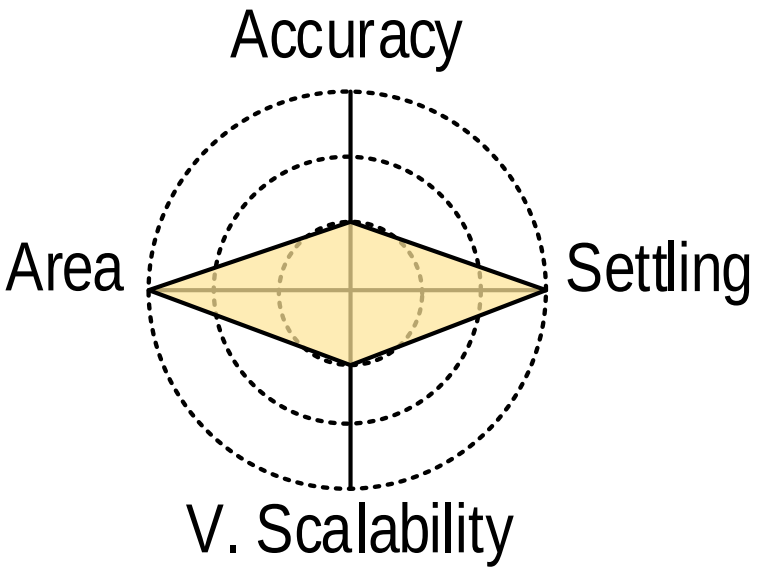


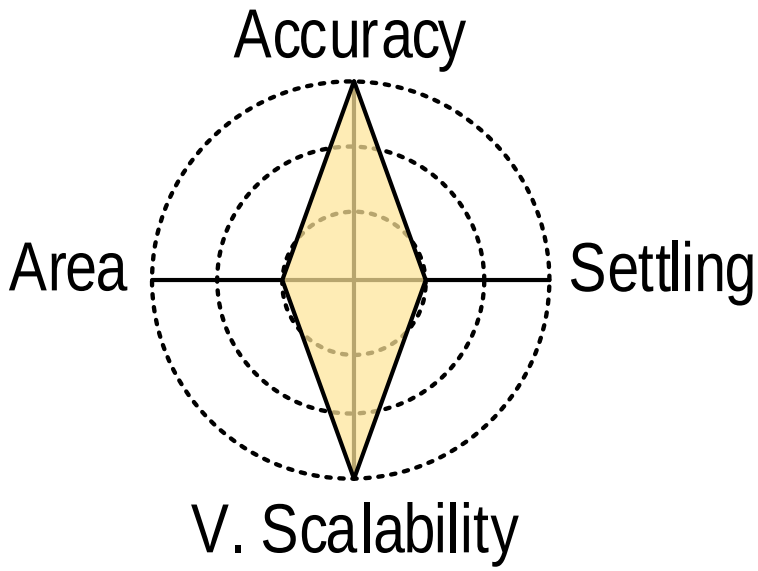
Frequency-Locked Loop



Truesdell, SSC-L'19







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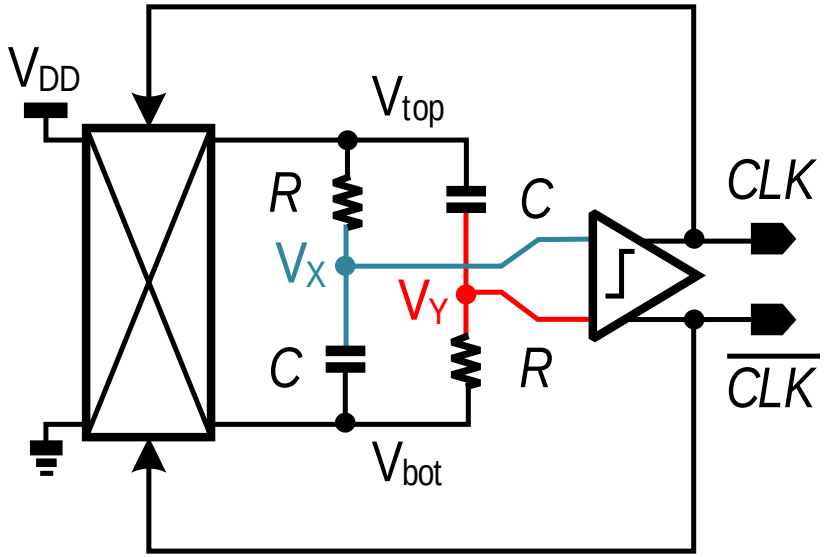
Simplified RxO Operation



Symmetric RC Network

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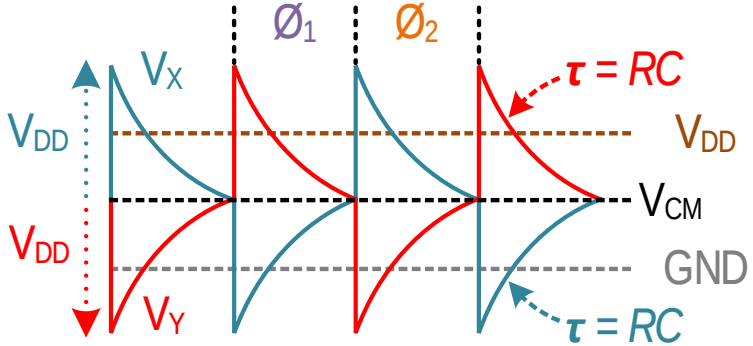
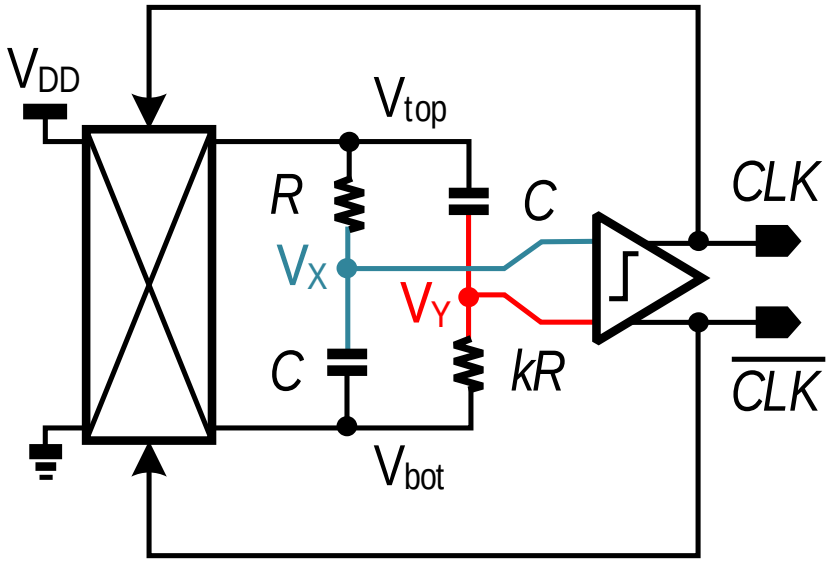


$V_{CM} = 0.5V_{DD}$

Simplified RxO Operation



Symmetric RC Network

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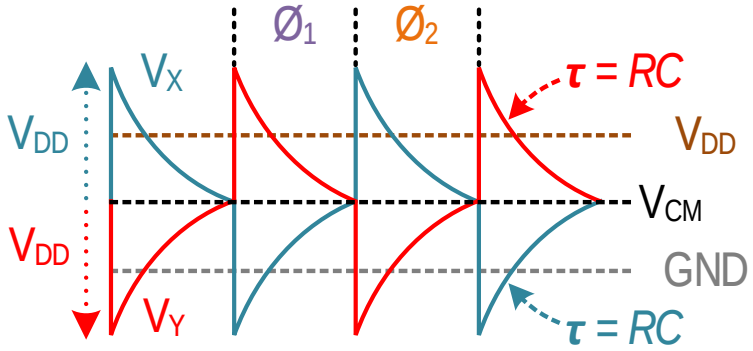
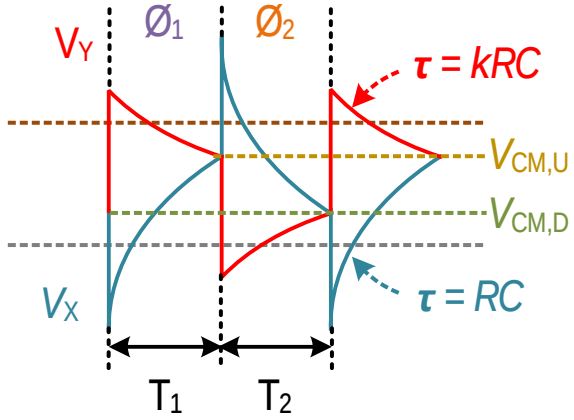


$V_{CM} = 0.5V_{DD}$

Asymmetric RC Network (k > 1)

[This work]



$V_{CM,U} > 0.5V_{DD}$ & $V_{CM,D} < 0.5V_{DD}$

Theoretical Analysis

$$\left(V_{CM,D}+V_{DD}\right)e^{-\frac{T_1}{kRC}}=V_{CM,U},$$

$$\left(V_{CM,D}-2V_{DD}\right)e^{-\frac{T_1}{RC}}+V_{DD}=V_{CM,U},$$

$$\left(V_{CM,U}+V_{DD}\right)e^{-\frac{T_2}{RC}}=V_{CM,D},$$

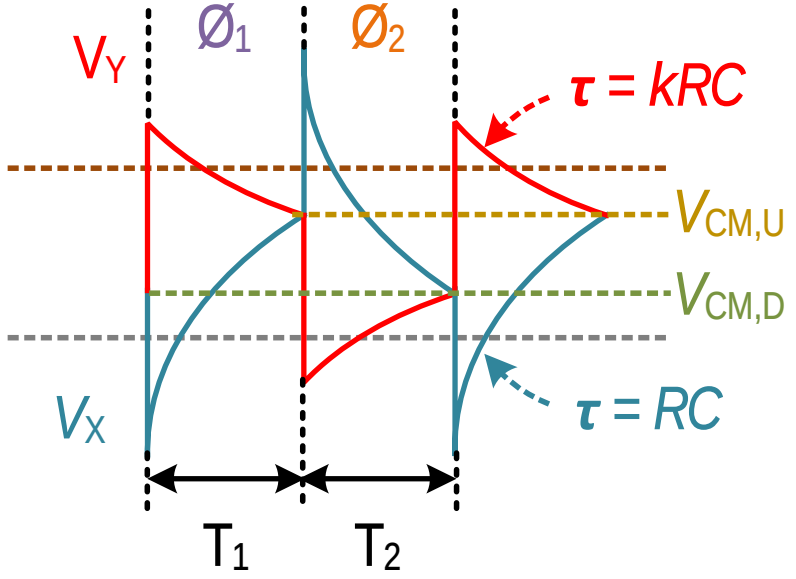
$$\left(V_{CM,U}-2V_{DD}\right)e^{-\frac{T_2}{kRC}}+V_{DD}=V_{CM,D}.$$

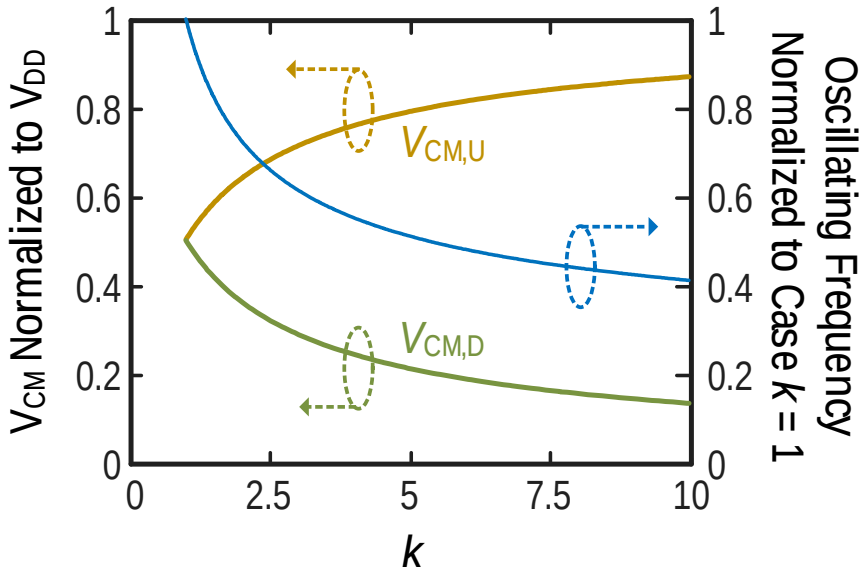
Assume T_1=T_2,

$$\left(\frac{V_{DD}-V_{CM,D}}{V_{DD}+V_{CM,D}}\right)^k=\frac{V_{CM,D}}{2V_{DD}-V_{CM,D}}$$

$$\left(\frac{V_{CM,U}}{2V_{DD}-V_{CM,U}}\right)^k=\frac{V_{DD}-V_{CM,U}}{V_{DD}+V_{CM,U}}$$

$$k=\frac{T}{2RC}/\ln\left(\frac{1+3e^{-T/2RC}}{1-e^{-T/2RC}}\right)$$



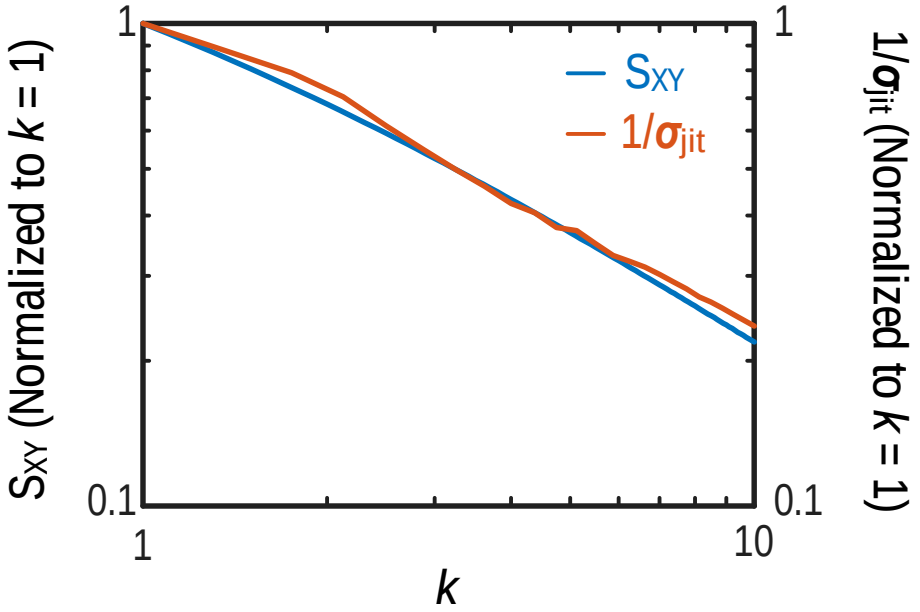


Theoretical Analysis

$$\sigma_{jit} \propto \frac{V_{n,xy}}{S_{xy}}$$

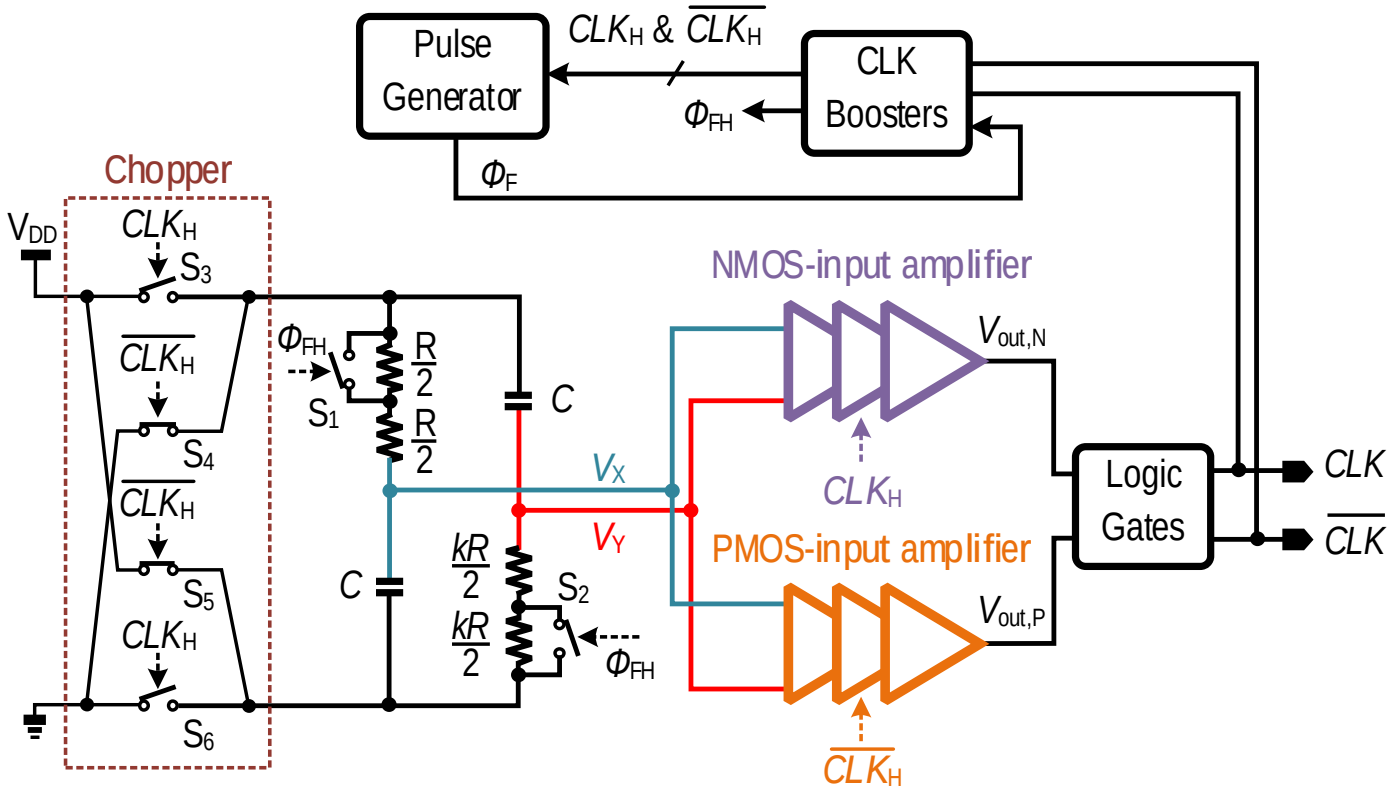
$$S_{xy} = \frac{dV_{x,y}}{dt}\left(t = \frac{T}{2}\right)$$

$$S_{xy} = -\frac{1}{RC}\left(V_{CM,D} - \frac{V_{CM,D}}{k} + \frac{V_{DD}}{k}\right)$$



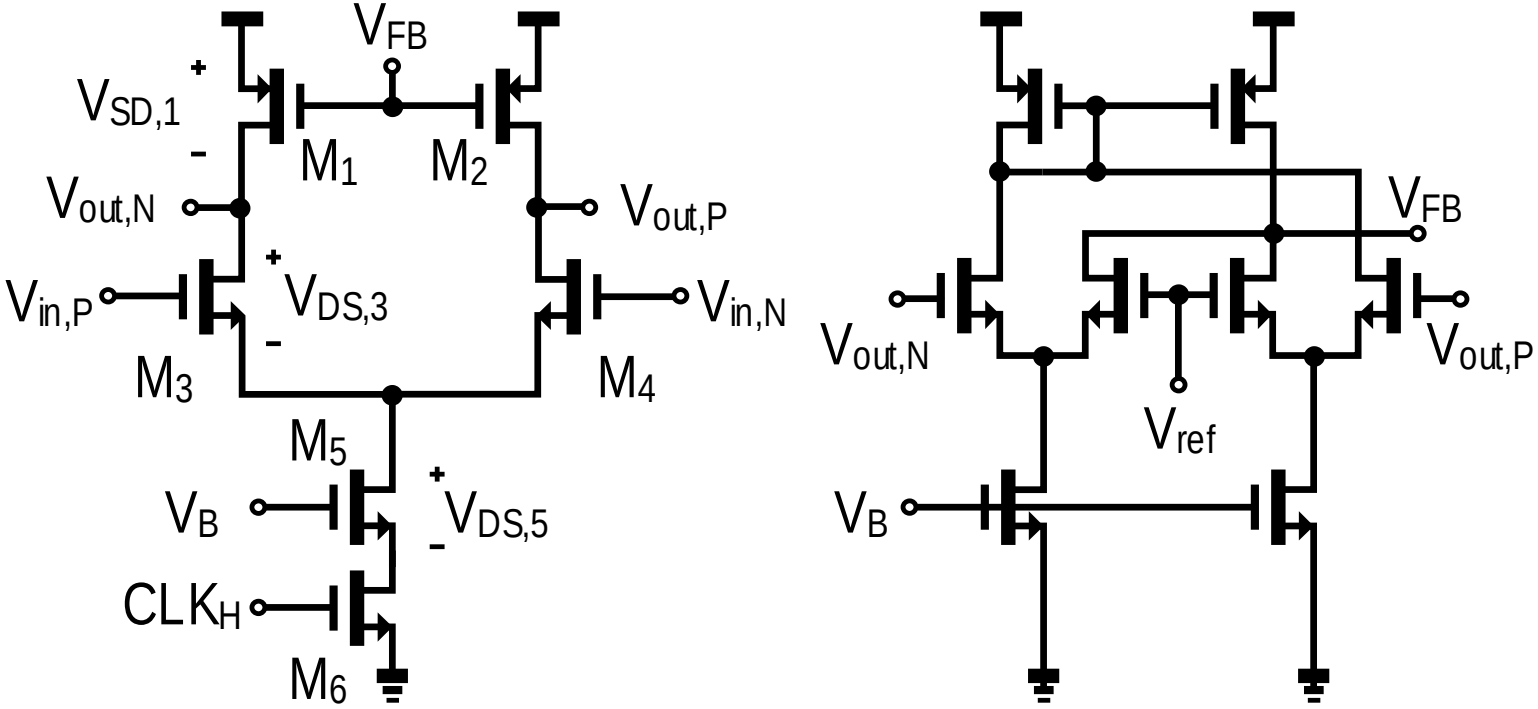
- Key takeaway:
  - A large *k* favors ULV design
  - A large *k* also penalizes the jitter
- k = 2.4 and $V_{CM,U}$ = 0.23 V (V_{DD}=0.35V).

Proposed ULV Dual-Path RxO



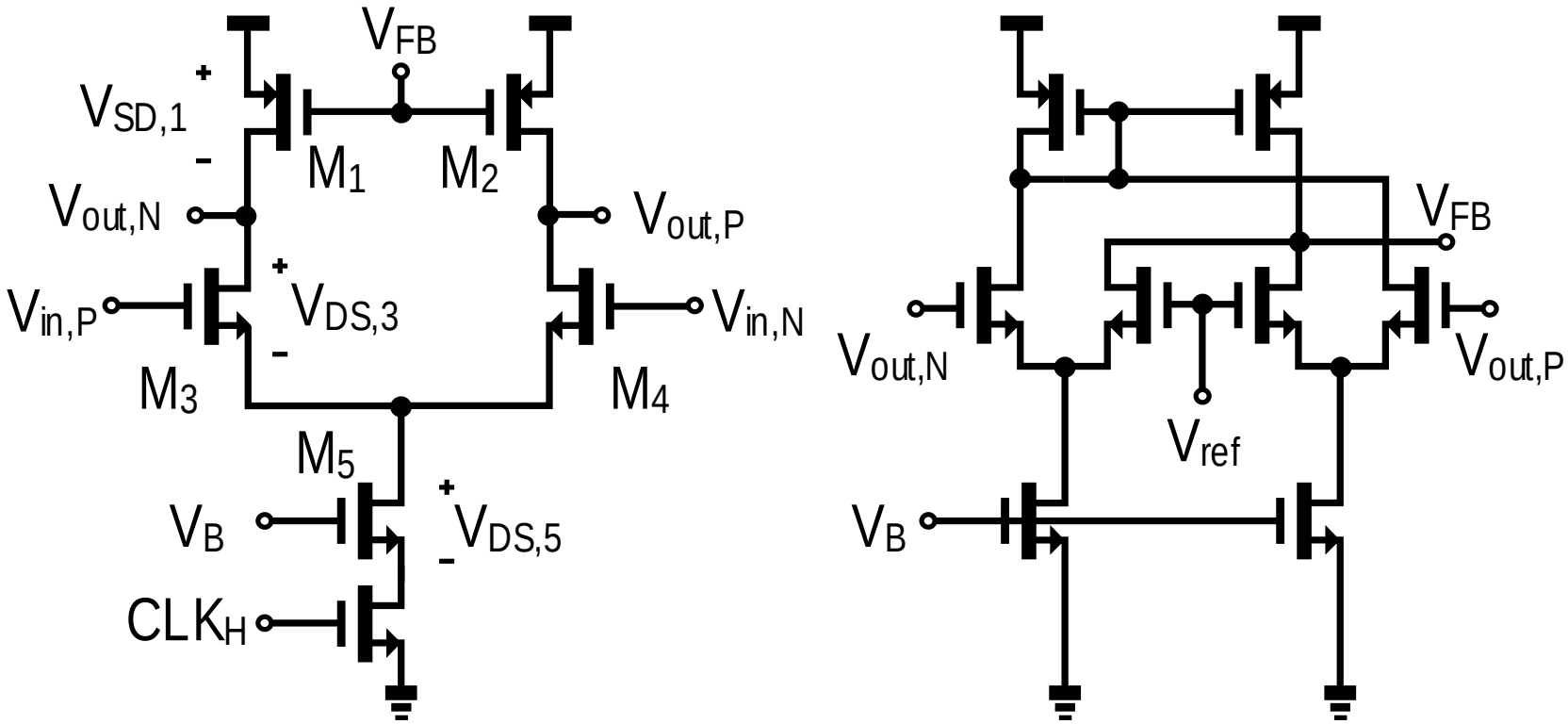
- NMOS-input + PMOS-input amp. for comparisons in $Ø_{1,2}$
- Logic gates to generate the CLK signals

Amplifier Implementation



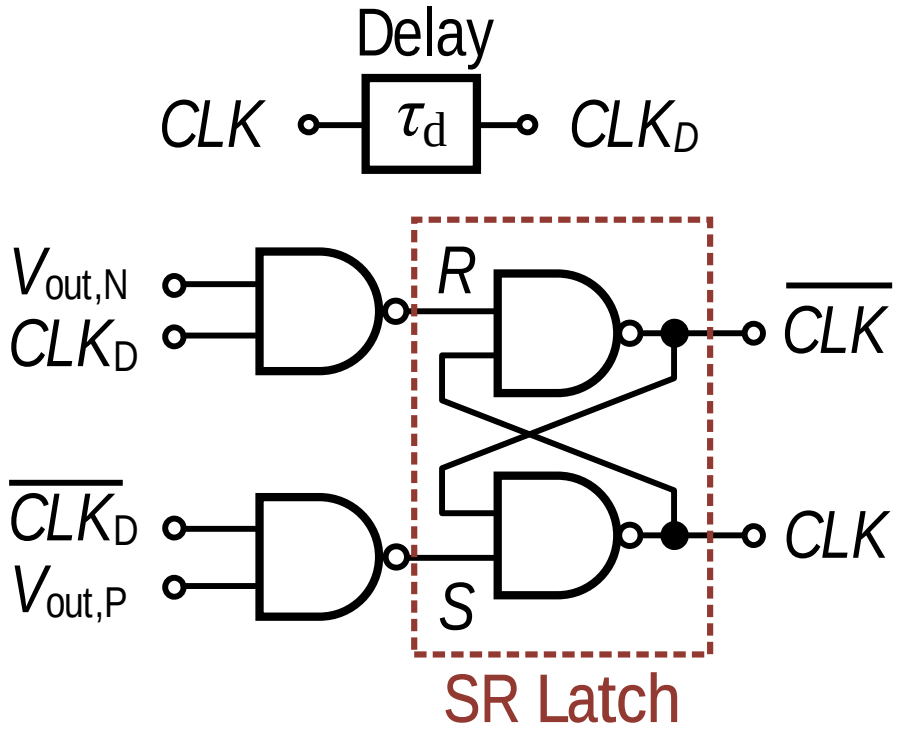
- 3 CS-amp. constitute the NMOS-/PMOS-input amp.
- Simulated gain: >27dB
- CMFB to safeguard the operation

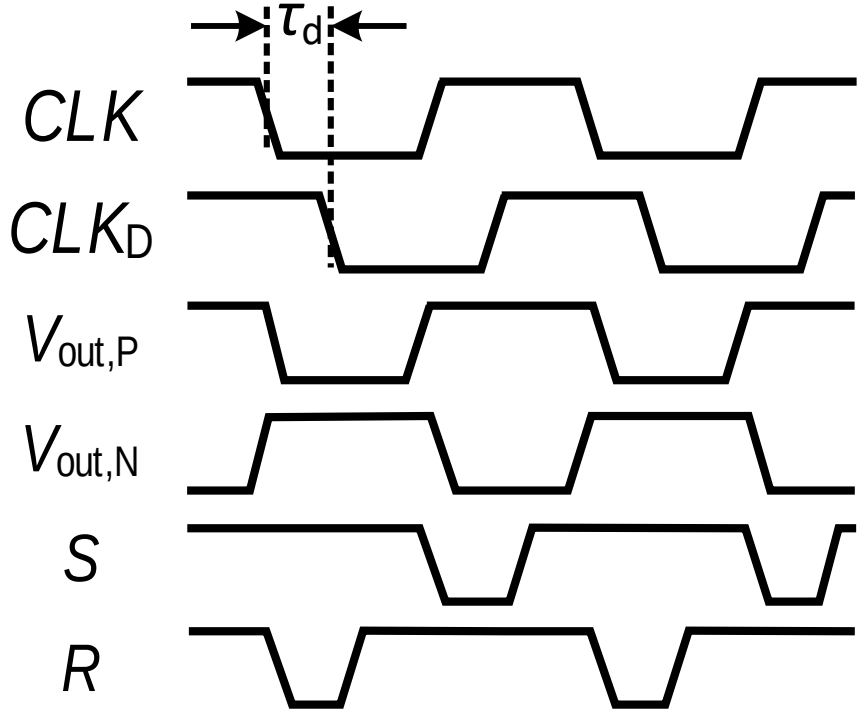
Amplifier Implementation



- Min. V_{DD} limited by comparator
  - $V_{SD,1} + V_{DS,3} + V_{DS,5}$
- $|V_{DS}| > 3V_T$ (V_T = 34mV @ 120°C)

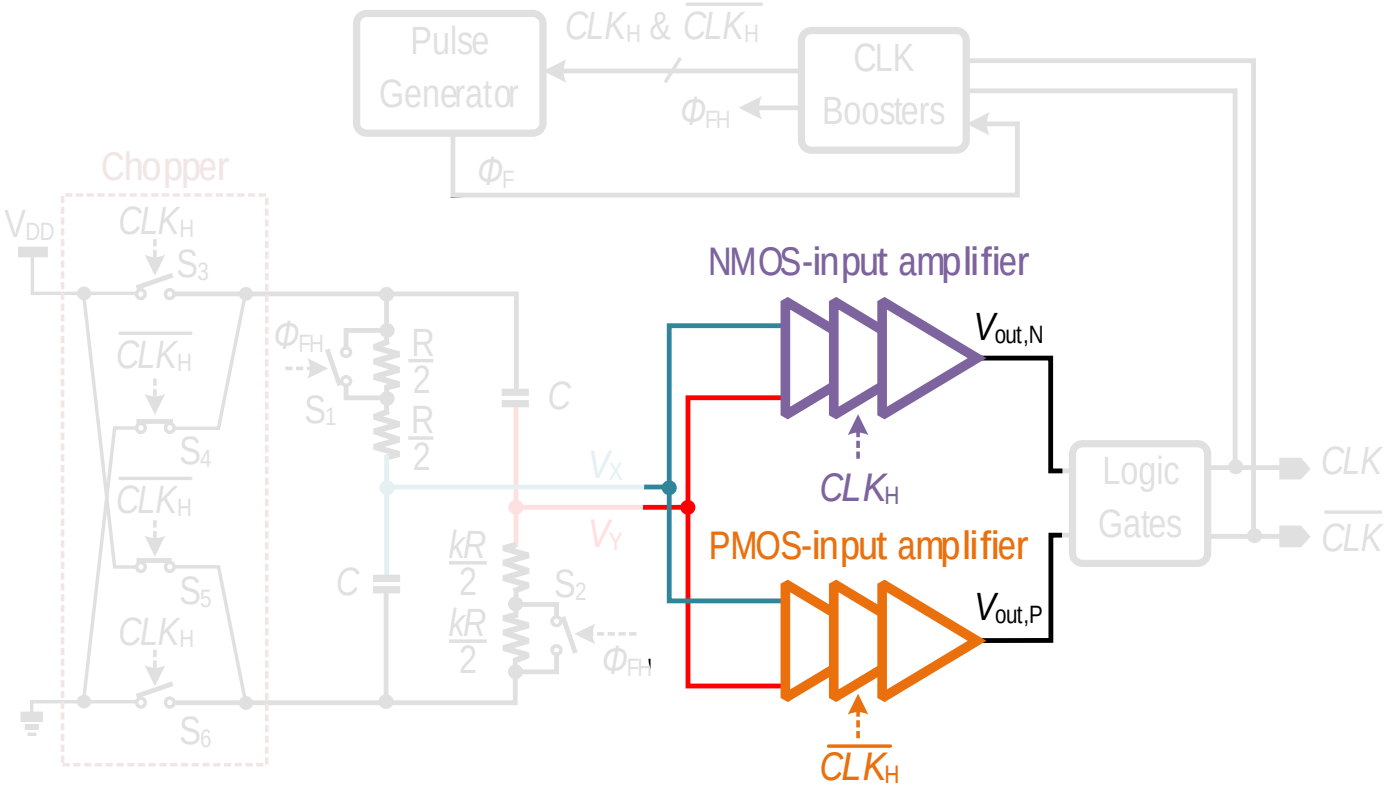
Logic Gates





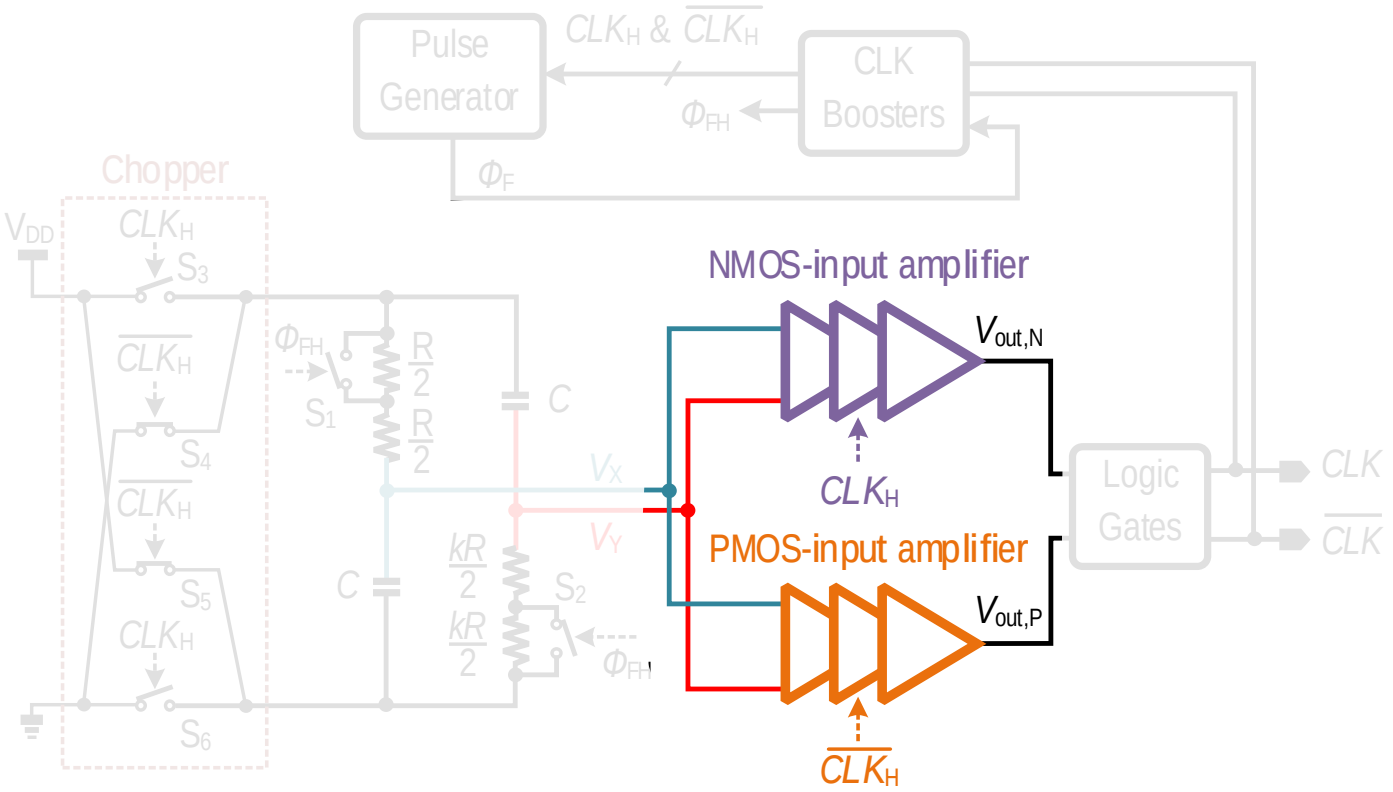
- Logic gates turn the output of amplifiers to CLK
- Delay cell to remove the undesired glitches
- Overall delay: vary <1% of the period from −20 to 120°C

Delay Compensation



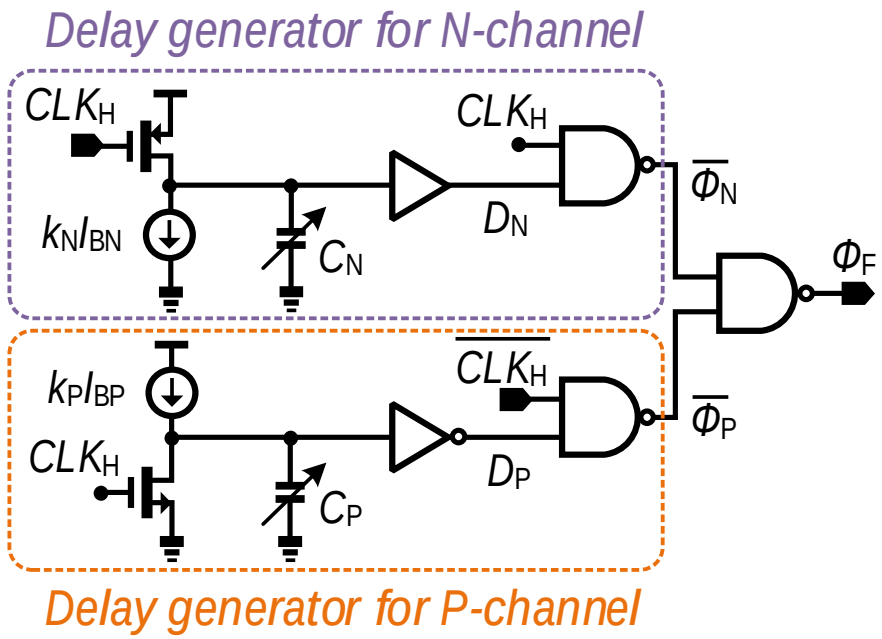
- Temperature-sensitive t_{delay} affects RxO's T_{OSC}
- Raising the amplifiers' power penalizes the efficiency

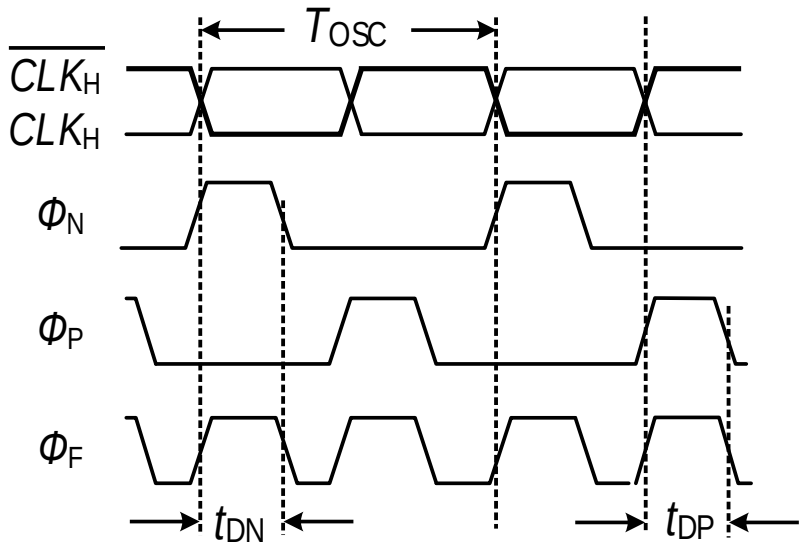
Delay Compensation

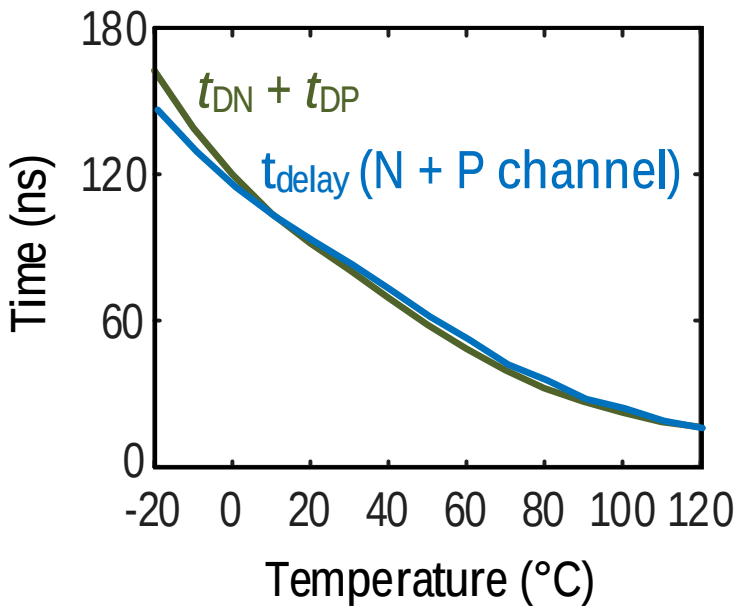


- Delay $\propto 1/I_{Bias}$
- Track the delay and compensate in the RC-network → Temperature-resilient operation

Delay Compensation

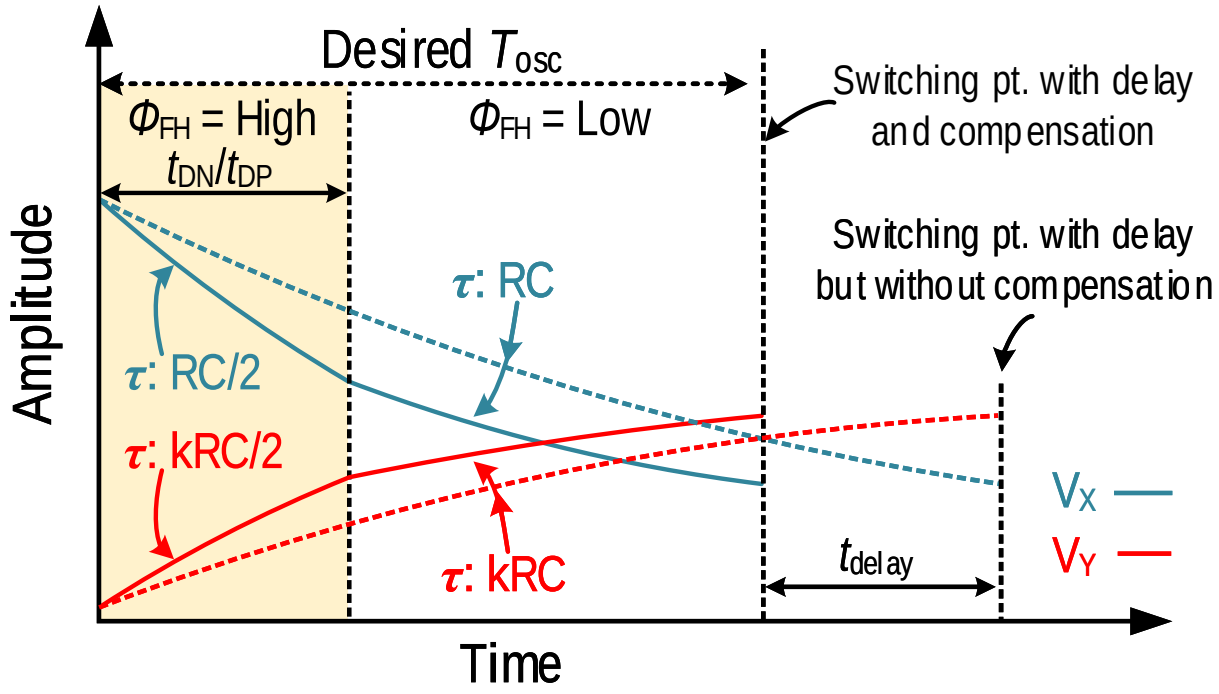


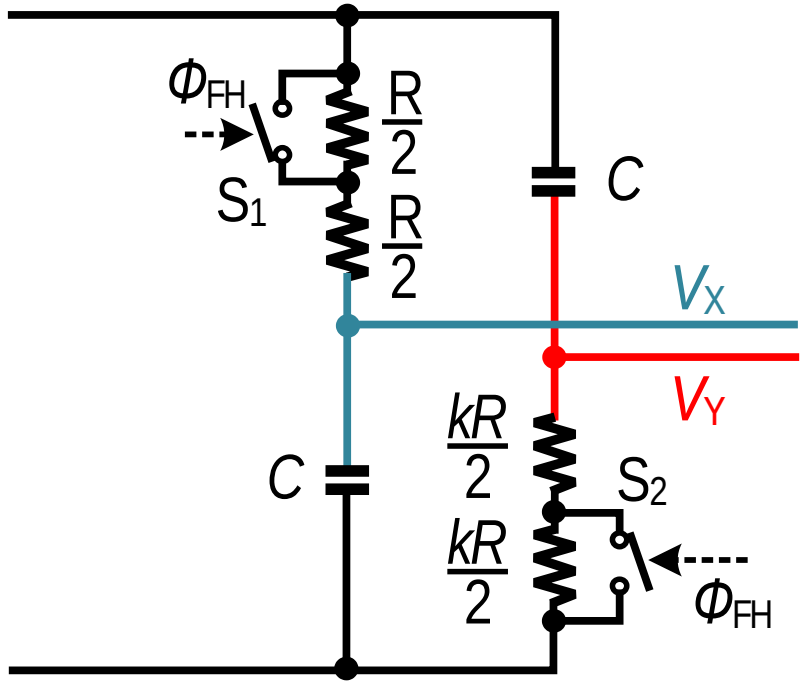




- Delay generators for both channels
- Pulse width inversely proportional to $I_{BN}//I_{BP}$

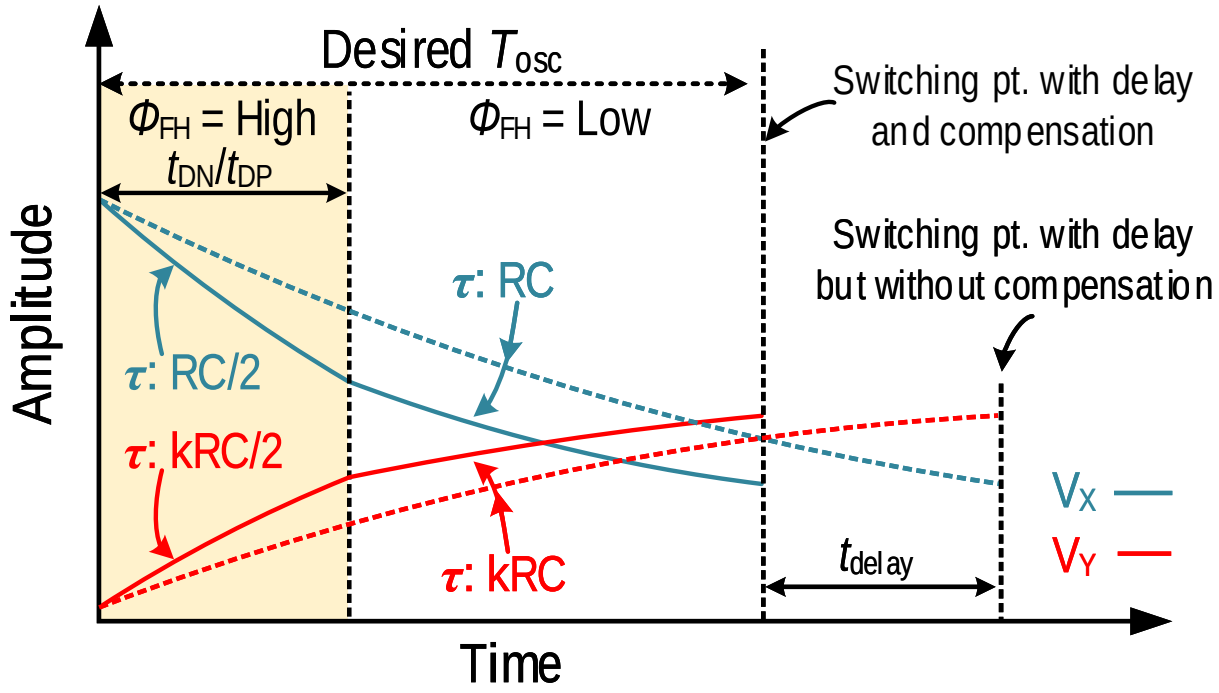
Delay Compensation

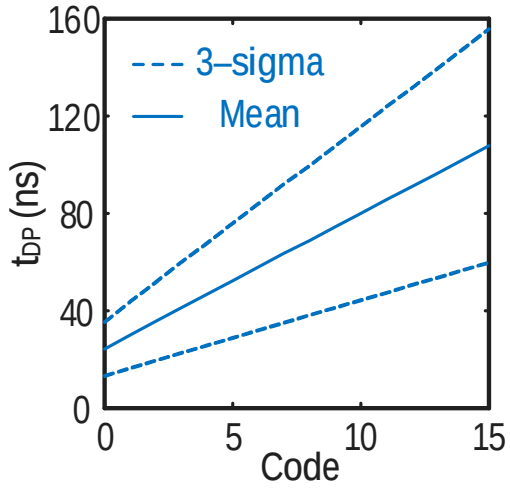


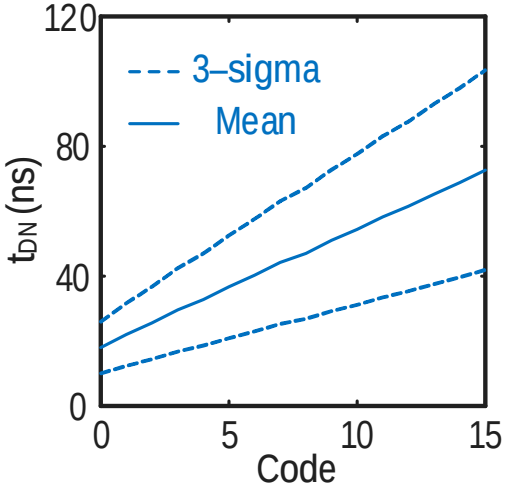


- τ of the RC branches is halved when $\emptyset_{FH} = 1$
- Mismatch/Process variations are calibrated through C_P and C_N

Delay Compensation







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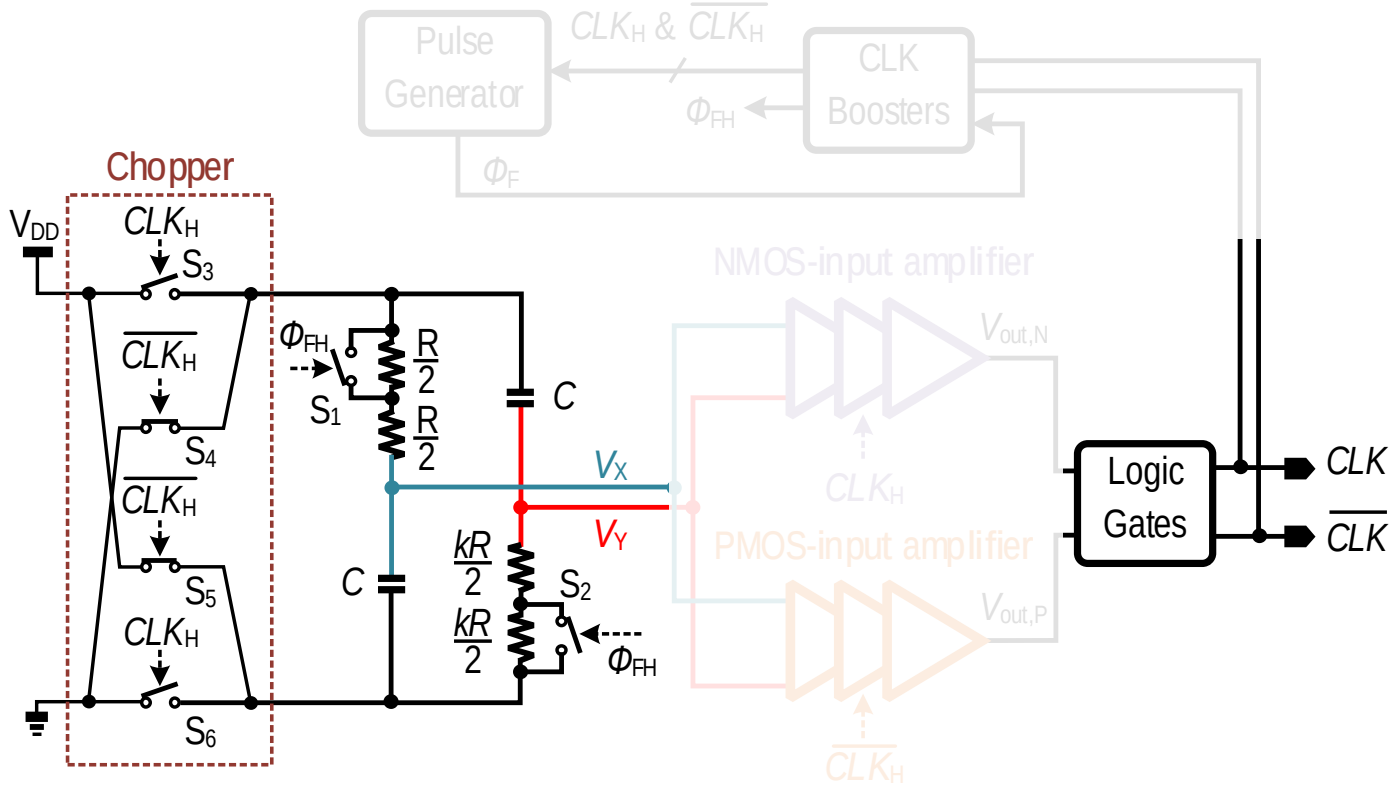
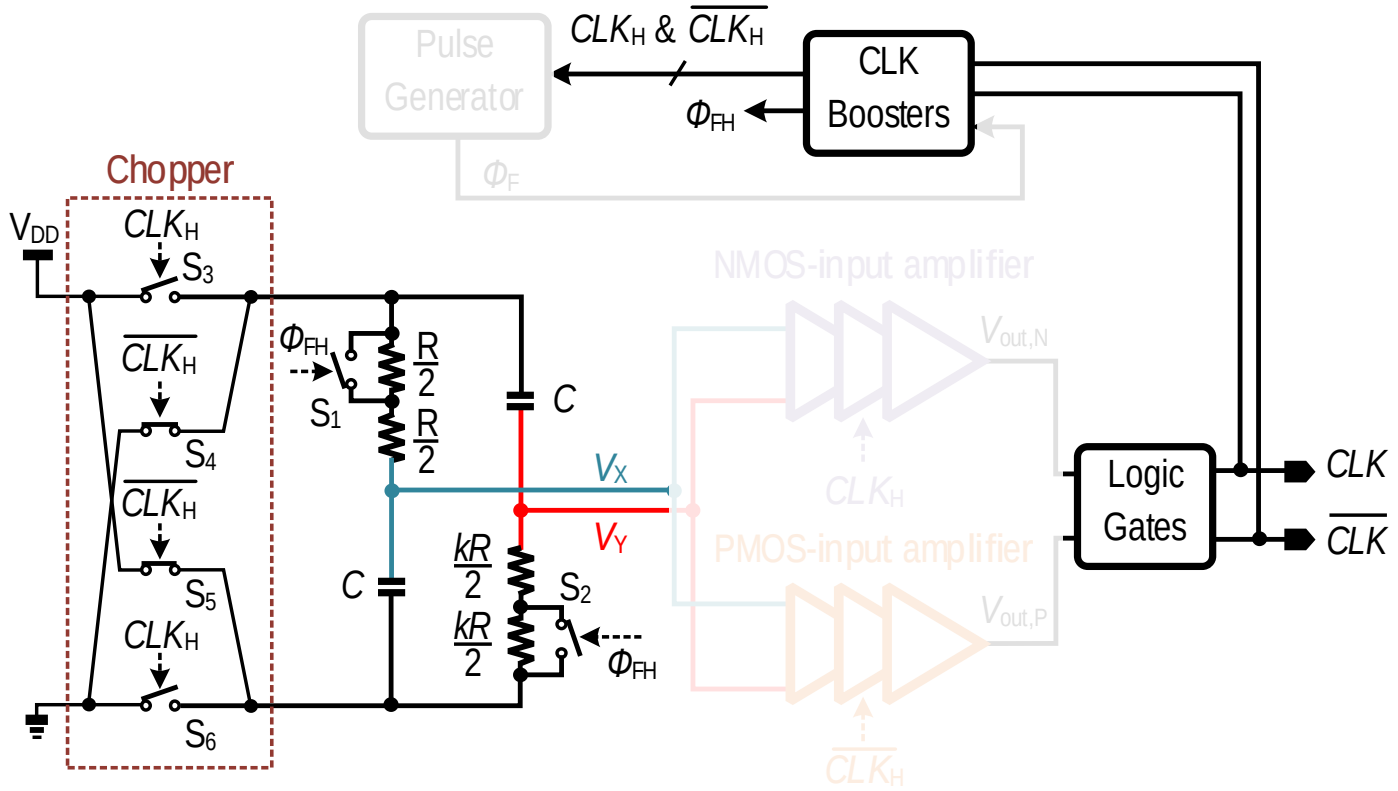
CLK Boosters



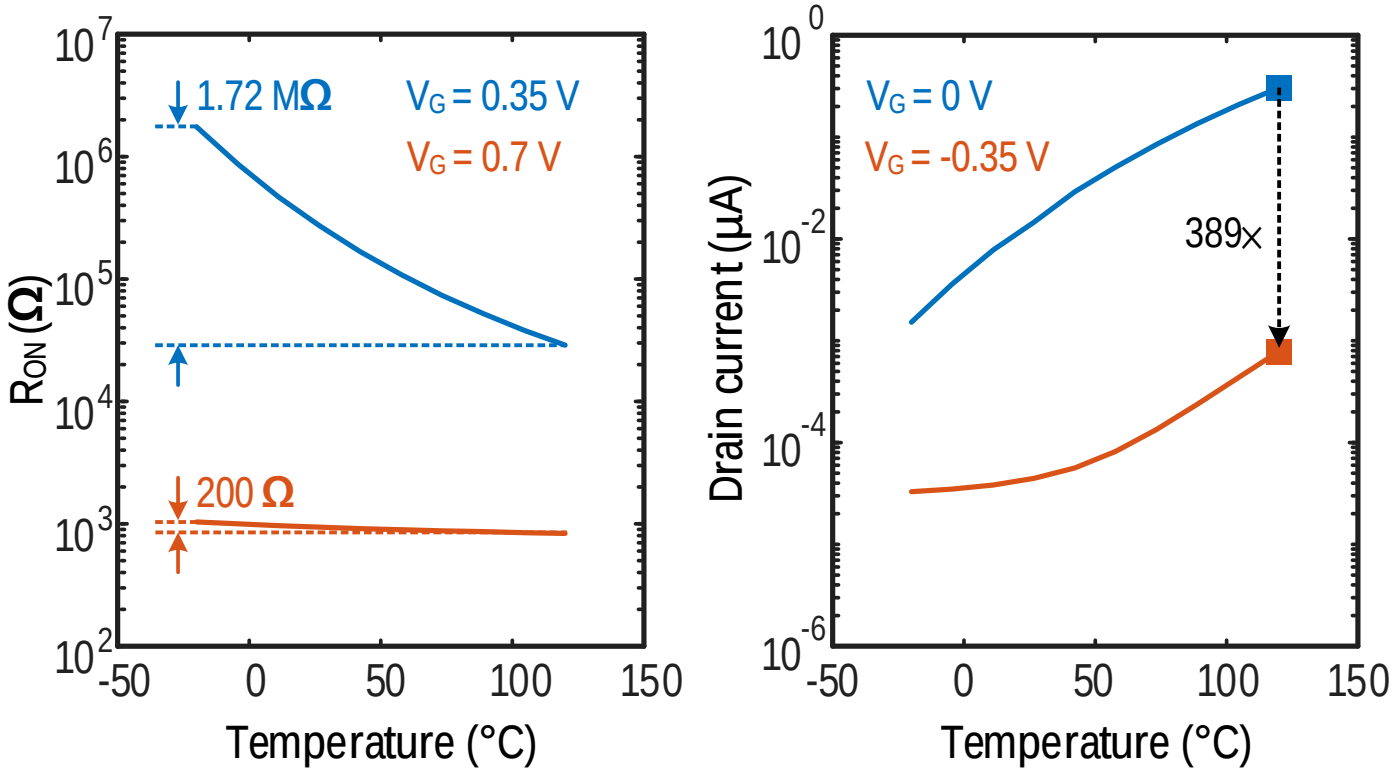
- R_{ON} of the switch is influential at 0.35V
- Leakage current of the switch also matters

CLK Boosters



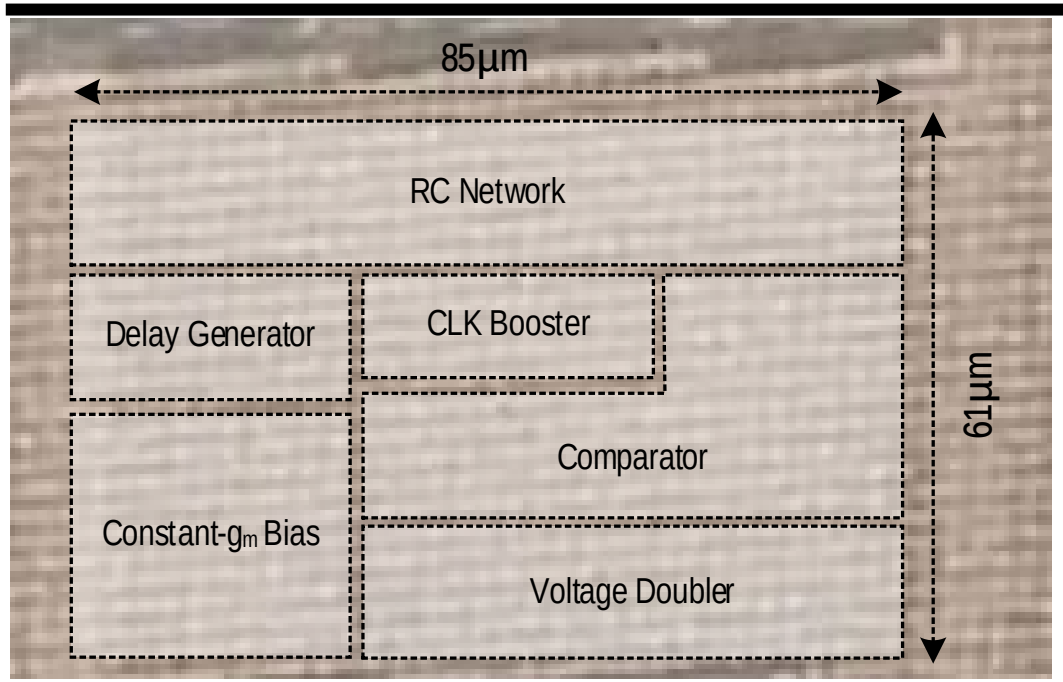
- CLK boosters to boost the swing ($3\times V_{DD}$)

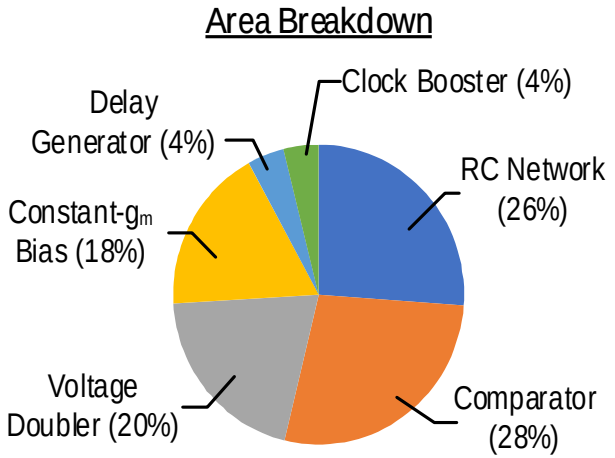
CLK Boosters

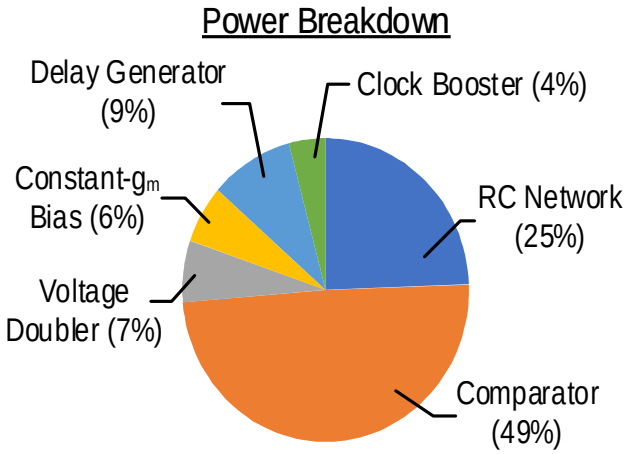


- Variations of R_{ON} (NMOS) reduced by 8600×
- Leakage current reduced from 307 to 0.8 nA at 120°C

Measurement Results

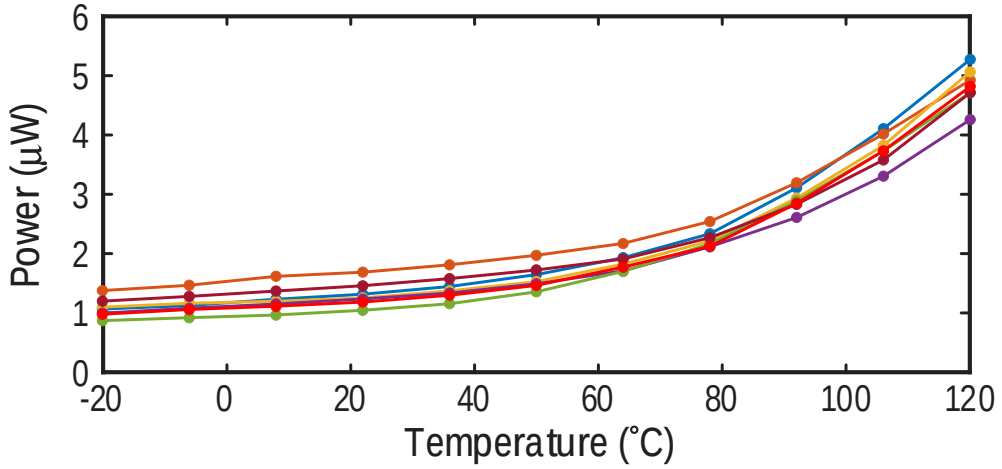


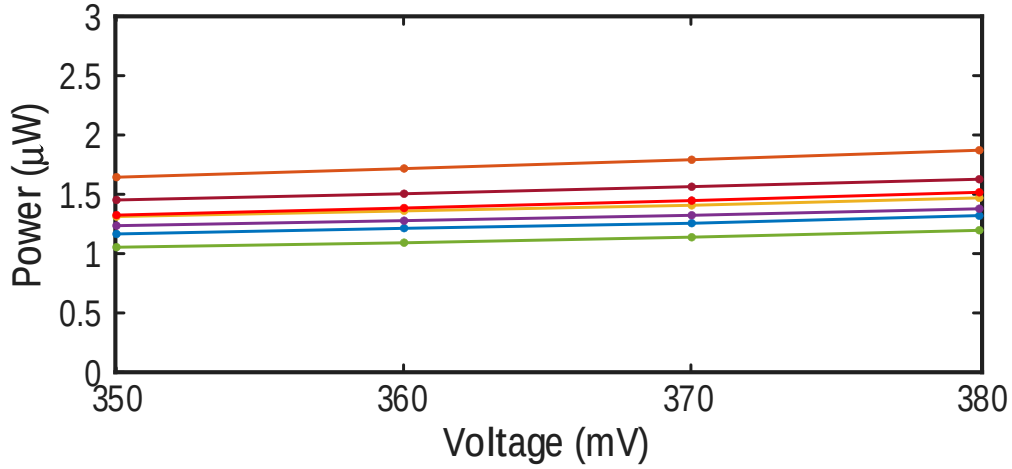


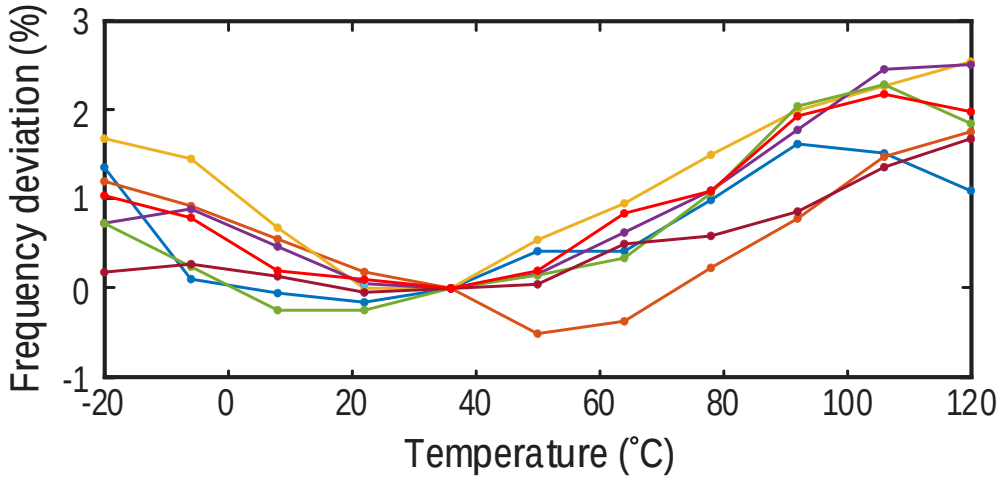


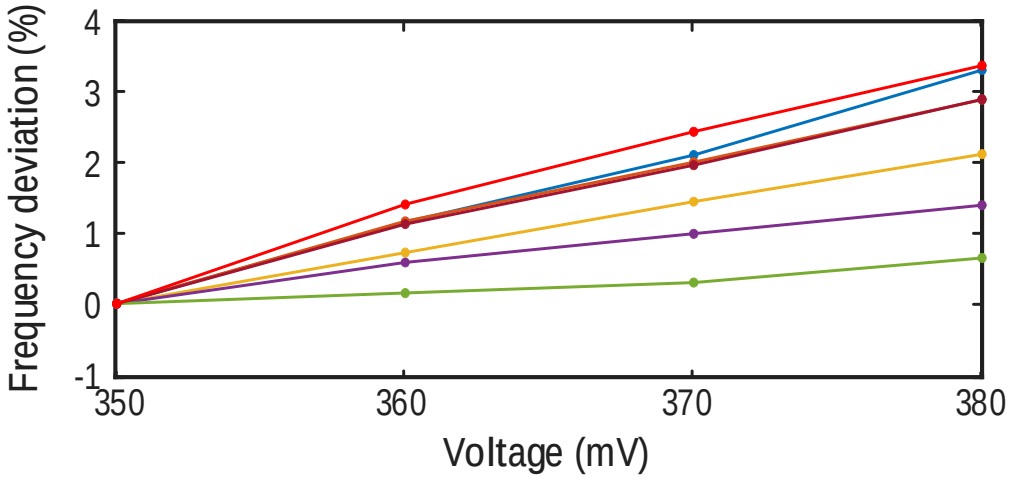
- Fabricated in 28-nm CMOS 1P10M process
- Area: 5,200µm^2
- P = 1.4 µW at 22 °C & f = 2.1 MHz (N = 7)
- Energy efficiency: 667fJ/cycle

Measurement Results



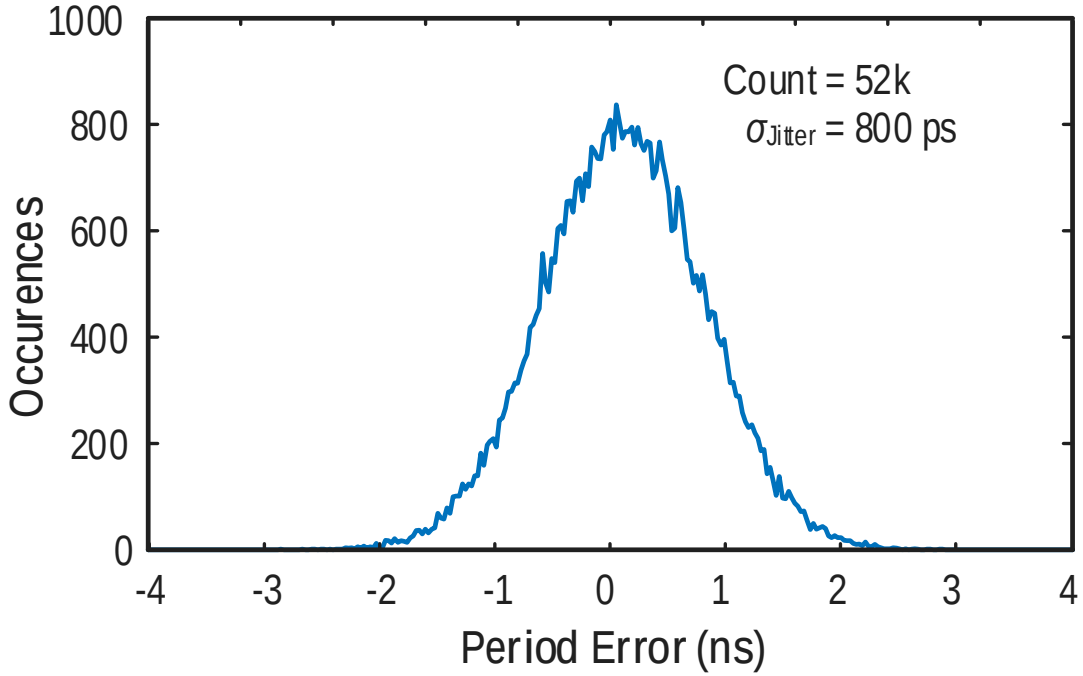


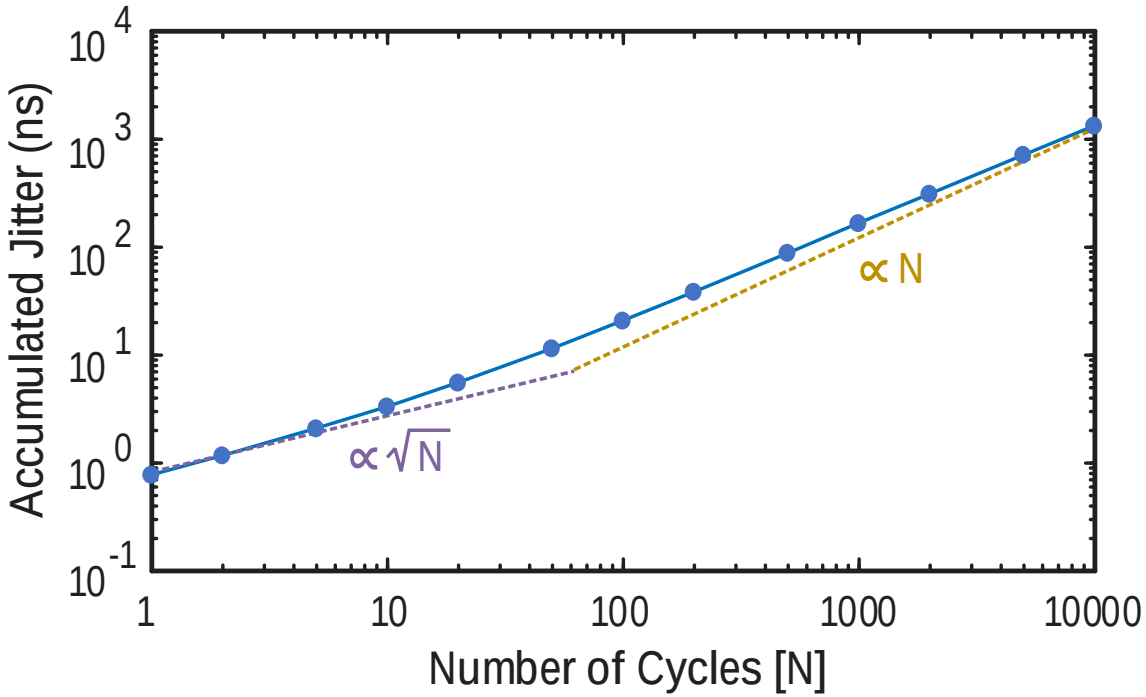




- TC: 158 ppm/°C
- $[(\frac{\Delta f}{f})/(\frac{\Delta V}{V})]$: 26.8%

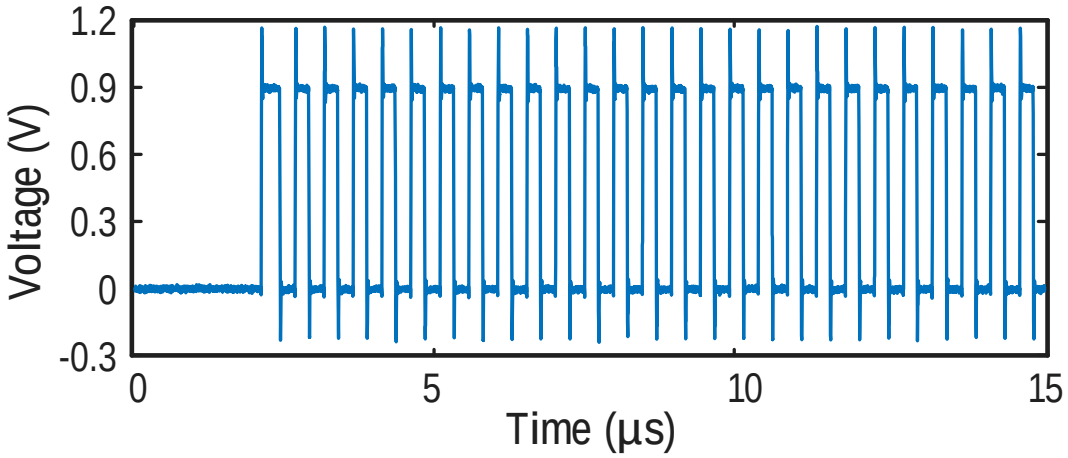
Measurement Results

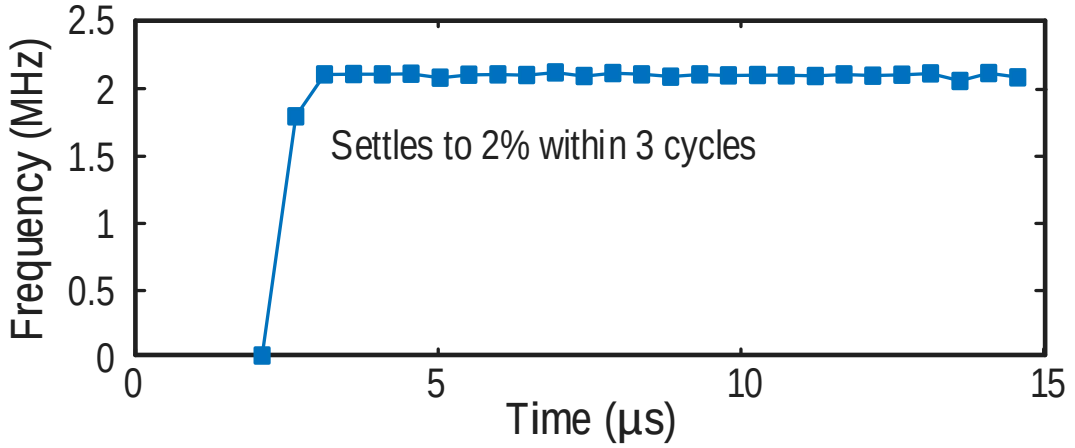




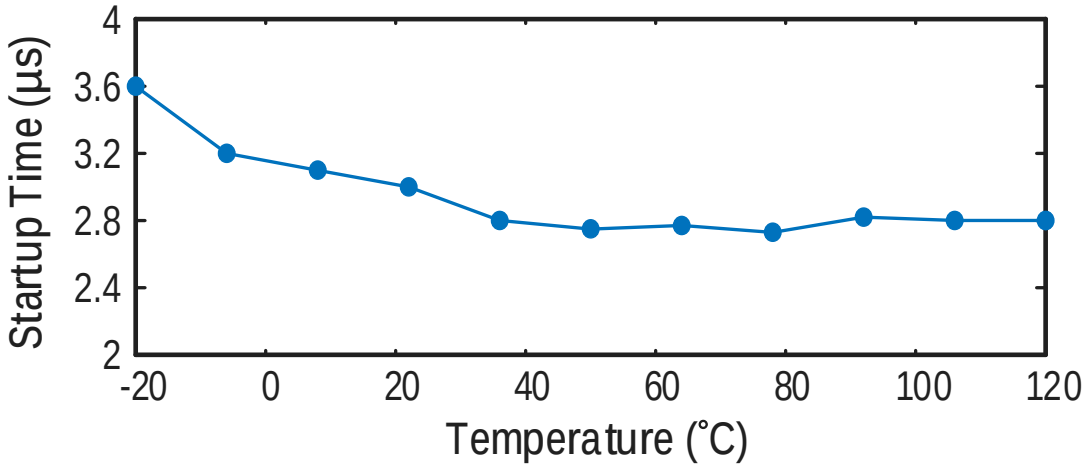
- RMS Jitter: 800 ps (0.15%)
- Accumulated jitter: increases $\propto \sqrt{N}$ up to ~60 cycles
- Long-term stability: 210 ppm (gating time > 0.1 s)

Measurement Results





- Settles in 3 cycles (<2%)
- <3.6µs in the entire T_{range}



Performance Summary and Comparison

	Koo, ISSCC'17 [11]	**Mikulić**, ESSCIRC'17 [8]	Liu, JSSC'19 [12]	Savanth, JSSC'19 [9]	Lee, JSSC'20 [13]	This work
Process (nm)	180	350	65	65	180	28
Frequency (MHz)	0.44	1	1.05	1.2	10.5	2.1
V_{DD} (V)	1.4 – 3.3	3 – 4.5	0.98 – 1.02	0.9 – 1.8	1.4 – 2.0	0.35 – 0.38
Power (µW)	21.3	210	69	0.82	219.8	1.4
Energy efficiency (pJ/cycle)	48.4	210	65.7	0.68	20.9	0.67
T_{range} (°C)	–20 to 100	–40 to 125	–15 to 55	–20 to 125	–40 to 125	–20 to 120
TC (ppm/°C)	169	24.3	4.3	100	137	158
Variation across V_{DD}	0.04%	0.42%	0.17%	±0.54%	2.64%	2.3%
Line sensitivity ($\frac{\Delta f}{f}/\frac{\Delta V}{V}$)	0.03%	0.84%	4.25%	±0.54%	6.16%	26.8%
Area (µm^2)	58,000	40,000	51,000	5,000	15,000	5,200
Period jitter (ps_{rms})	1,060	-	160	-	9.86	800
Startup time (µs)	-	1[§]	8	10	-	3.6
No. of samples	100	5	-	7[#]	15	7
FoM_1 (dB)▲	162	165	174	183	168	181
FoM_2 (dBc/Hz)♣	–152.7 (@10 kHz)	-	-	-	–157.7 (@1 kHz)	–143.4 (@ 10 kHz)

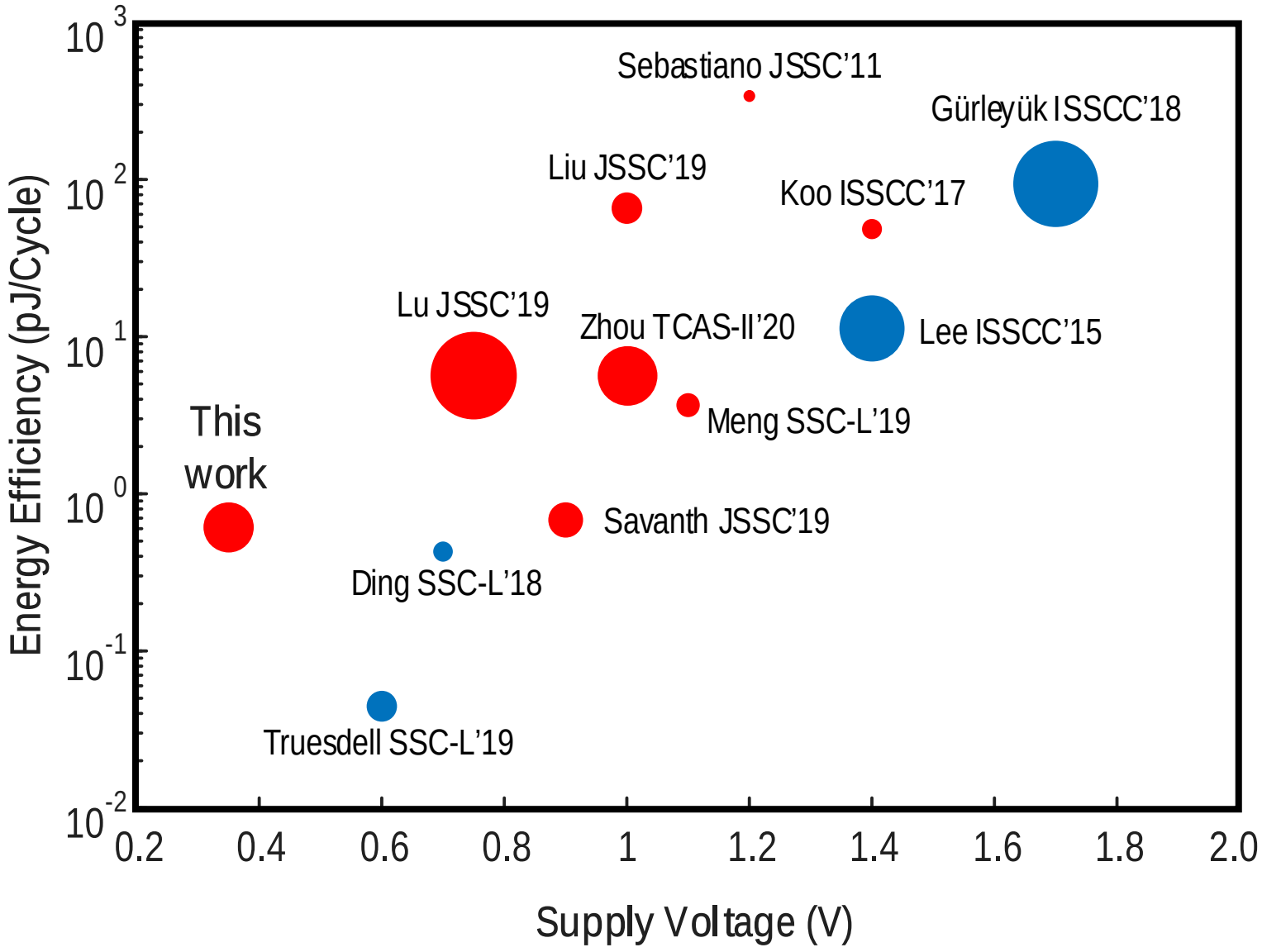
[#]For temperature stability measurement.

[§]Deduced from the numbers of cycles to start, which may underestimate the true startup time.

▲$FoM_1 = 10\log(\frac{f \cdot T_{range}}{Power \cdot TC})$

♣$FoM_2 = PN - 20\log\left(\frac{f}{f_{offset}}\right) + 10\log(\frac{Power}{1mW})$

Comparison with State-of-the-art



Conclusion

- 2.1-MHz and 0.35-V ULV RxO in 28-nm CMOS
- Asymmetric RC-network to shift $V_{CM,D}$ and $V_{CM,U}$
- Dual-path comparator for comparison
- Open-loop delay generator to compensate the delay
- Active Area: 5,200 μm^2
- Energy efficiency: 667 fJ/cycle
- FoM_1: 181dB
- **A promising solution for ULV and ULP IoT timer**

Acknowledgement

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The End